CLAIMS

I Claim:

1. A power amplifier capable of operating in a high power mode and a low power mode, the power amplifier comprising:

a first amplifier output stage configured to receive a radio frequency (RF) input signal, wherein the first amplifier output stage is enabled during both the high power mode and the low power mode;

a second amplifier output stage configured to receive the RF input signal; and

a control circuit coupled to the second amplifier output stage, wherein the control circuit is configured to enable the second amplifier output stage during the high power mode, and wherein the control circuit is configured to disable the second amplifier output stage during the low power mode.

2. The power amplifier of Claim 1, wherein the power amplifier is capable of operating in an intermediate power mode between the high power mode and the low power mode, the power amplifier further comprising:

a third amplifier output stage configured to receive the RF input signal; and

a second control circuit coupled to the third amplifier output stage, wherein the second control circuit is configured to enable the third amplifier output stage during the high power mode, and wherein the second control circuit is configured to disable the third amplifier output stage during the intermediate power mode.

3. The power amplifier of Claim 1, wherein the first amplifier output stage comprises:

a first set of transistors, each having a control electrode coupled to receive the RF input signal;

a first set of distributed bias circuits, wherein the control electrode of each of the transistors in the first set of transistors is coupled to a corresponding distributed bias circuit in the first set of distributed bias circuits; and

a first common bias reference circuit coupled to each of the distributed bias circuits in the first set of distributed bias circuits.

4. The power amplifier of Claim 3, wherein the second amplifier output stage comprises:

a second set of transistors, each having a control electrode coupled to receive the RF input signal;

a second set of distributed bias circuits, wherein the control electrode of each of the transistors in the second set of transistors is coupled to a corresponding distributed bias circuit in the second set of distributed bias circuits; and

a second common bias reference circuit coupled to each of the distributed bias circuits in the second set of distributed bias circuits.

5. The power amplifier of Claim 4, wherein there are more transistors in the second set of transistors than in the first set of transistors.

6. The power amplifier of Claim 4, wherein the first set of distributed bias circuits and the first common bias

reference circuit form a first set of temperature adaptive bias circuits, and wherein the second set of distributed bias circuits and the second common bias reference circuit form a second set of temperature adaptive bias circuits.

7. The power amplifier of Claim 1, wherein the second amplifier output stage comprises:

a plurality of transistors, each having a control electrode coupled to receive the RF input signal; and

a bias reference circuit configured to provide DC bias voltages to the control electrodes of each of the plurality of transistors.

8. The power amplifier of Claim 7, wherein the control circuit comprises circuitry for forcing the DC bias voltages to a level that will turn off the plurality of transistors.

9. The power amplifier of Claim 7, wherein the bias reference circuit comprises a common bias reference circuit that is common to each of the plurality of transistors, and a plurality of distributed bias circuits, each associated with a corresponding one of the plurality of transistors.

10. The power amplifier of Claim 1, further comprising an amplifier input stage configured to receive a primary RF signal and in response, provide the RF input signal.

11. A method of operating a power amplifier comprising:

receiving a radio frequency (RF) input signal with a first amplifier output stage and a second amplifier

output stage;

enabling the first amplifier output stage and disabling the second amplifier output stage during a low power operating mode of the power amplifier; and

enabling the first amplifier output stage and the second amplifier output stage during a high power operating mode of the power amplifier.

12. The method of Claim 11, further comprising:

receiving the RF input signal with a third amplifier output stage;

disabling the third amplifier output stage during the low power operating mode of the power amplifier;

enabling the third amplifier output stage during the high power operating mode of the power amplifier; and

enabling the first amplifier output stage and the third amplifier output stage, and disabling the second amplifier output stage during an intermediate power operating mode of the power amplifier.

13. The method of Claim 11, further comprising:

biasing a first set of transistors in the first amplifier output stage with a common bias reference circuit and a plurality of distributed bias circuits; and

biasing a second set of transistors in the second amplifier output stage with a common bias reference circuit and a plurality of distributed bias circuits.

14. The method of Claim 11, wherein there are more transistors in the second set of transistors than in the

first set of transistors.

15. The method of Claim 11, further comprising:

biasing a first set of transistors in the first amplifier output stage in a temperature adaptive manner; and

biasing a second set of transistors in the second amplifier output stage in a temperature adaptive manner.

16. A power amplifier capable of operating in a high power mode and a low power mode, the power amplifier comprising:

a first amplifier output stage configured to receive a radio frequency (RF) input signal;

a second amplifier output stage configured to receive the RF input signal;

means for enabling the first amplifier output stage during the low power mode and the high power mode; and

means for enabling the second amplifier output stage during the high power mode, and disabling the second amplifier output stage during the low power mode.

17. The power amplifier of Claim 16, further comprising:

means for biasing a first set of transistors in the first amplifier output stage with a common bias reference circuit and a plurality of distributed bias circuits; and

means for biasing a second set of transistors in

the second amplifier output stage with a common bias reference circuit and a plurality of distributed bias circuits.

18. The power amplifier of Claim 16, wherein the first amplifier output stage comprises a first set of transistors having control electrodes configured to receive the RF input signal and the second amplifier output stage comprises a second set of transistors having control electrodes configured to receive the RF input signal, wherein there are more transistors in the second set of transistors than in the first set of transistors.

19. The power amplifier of Claim 16, further comprising:

means for biasing a first set of transistors in the first amplifier output stage in a temperature adaptive manner; and

means for biasing a second set of transistors in the second amplifier output stage in a temperature adaptive manner.

20. A power amplifier capable of operating in a high power mode an intermediate power mode and a low power mode, the power amplifier comprising:

a first amplifier output stage configured to receive a radio frequency (RF) input signal;

a second amplifier output stage configured to receive the RF input signal;

a third amplifier output stage configured to receive the RF input signal;

means for enabling the first amplifier output

stage during the low power mode, the intermediate power mode and the high power mode;

means for enabling the second amplifier output stage during the high power mode, and disabling the second amplifier output stage during the low power mode and the intermediate power mode; and

means for enabling the third amplifier output stage during the high power mode and the intermediate power mode, and disabling the second amplifier output stage during the low power mode.